## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An article comprising a machine-accessible medium having stored thereon instructions that, when executed by a machine, cause the machine to:

obtain from a performance monitor ~~data on~~ runtime performance data of a thread level utilization, wherein the runtime performance data ~~being~~ is indicative of a set of execution characteristics of the thread including an ~~instructions per clock~~ instructions-per-clock cycle metric and ~~including~~ a [[memory references-per-cycle]] memory references-per-clock cycle metric, wherein the runtime performance data includes instruction counts, memory references and cycle counts obtained from a timer interrupt in the performance monitor; and

based on the runtime performance data, adjust an operating voltage or an operating frequency of the machine, wherein the operating voltage and operating frequency are nonzero.

2. (Currently amended) The article of claim 1, wherein the performance monitor is a Performance Monitoring Unit (PMU) and is part of a central processing unit (CPU) within the machine.

3. (Canceled)

4. (Currently amended) The article of claim [[2]] 5, wherein the PMU includes a plurality of counters for simultaneously measuring multiple different performance data.

5. (Currently amended) The article of claim [[1]] 2, wherein the runtime performance data includes at least one from the group consisting of instruction cache misses, data cache misses, instructions executed, branches executed, branch mis-predicts, instruction translation look-up buffer TLB misses, data translation look-up buffer TLB misses, stalls due to data dependency, and data cache write-backs.

6. (Currently amended) The article of claim 1, having further instructions that, when executed by the machine, cause the machine to:

in response to the runtime performance data, determine if the operating voltage and operating frequency should be adjusted upward or scaled down.

7. (Currently amended) The article of claim 6, having further instructions that, when executed by the machine, cause the machine to:

compare the runtime performance data to a voltage and frequency scheduler lookup table that stores at least one voltage value and at least one frequency value.

8. (Currently amended) The article of claim 1, having further instructions that, when executed by the machine, cause the machine to:

simultaneously obtain a plurality of runtime performance data; and

in response to the plurality of runtime performance data, adjusting the operating voltage and the operating frequency.

9. (Canceled)

10. (Canceled)

11. (Original) The article of claim 1, having further instructions that, when executed by the machine, cause the machine to:

operate the performance monitor in an operating system environment in communication with a platform hardware environment, in a kernel mode, and in communication with an end user code, in a user mode.

12. (Original) The article of claim 1, wherein the instructions, when executed by the machine, cause the machine to adjust the operating voltage and the operating frequency.

13. (Currently Amended) A method comprising:

obtaining, from a performance monitor, ~~data on~~ runtime performance data of a thread level utilization, the runtime performance data being indicative of a set of execution characteristics of a thread, including an ~~instructions-per-clock-cycle~~ instructions-per-clock cycle metric and a memory references-per-clock cycle metric[[,]] for a central processing unit (CPU) having an operating voltage and an operating frequency;

in response to the runtime performance data, determining if either the operating voltage or the operating frequency is at a desired value; and

in response to the determination, adjusting the operating voltage or the operating frequency in response to the [[instructions-per-cycle]] instructions-per-clock cycle metric and [[a]] the [[memory-references-per-cycle]] memory references-per-clock cycle metric, wherein the operating voltage and operating frequency are nonzero.

14. (Original) The method of claim 13, further comprising:
adjusting both the operating voltage and the operating frequency.

15. (Original) The method of claim 14, further comprising adjusting the operating voltage and the operating frequency upward.

16. (Original) The method of claim 14, further comprising adjusting the operating voltage and the operating frequency downward.

17. (Original) The method of claim 13, wherein the performance monitor is a Performance Monitoring Unit (PMU).

18. (Previously presented) The method of claim 13, wherein the runtime performance data includes at least one from the group consisting of instruction cache misses, data cache misses, instructions executed, branches executed, branch mis-predicts, instruction translation look-up buffer misses, data translation look-up buffer misses, stalls due to data dependency, and data cache write-backs.

19. (Original) The method of claim 13, further comprising comparing the performance data to a voltage and frequency scheduler lookup table that includes at least one voltage value and at least one frequency value.

20. (Original) The method of claim 19, further comprising:

benchmarking the CPU;

determining the at least one voltage value and the at least one frequency value in response to the benchmarking; and

creating a lookup table of the at least one voltage value and the at least one frequency value.

21. (Canceled)

22. (New) A method for adjusting operating voltage and/or operating frequency on a machine having a processor, the method comprising:

the machine simultaneously monitoring multiple performance events, where each performance event reflects a different thread level utilization of at least one application executing on the processor;

based on the simultaneously monitored multiple performance events, obtaining multiple performance metrics indicating events per clock cycle of the at least one executing application; and

based on the multiple performance metrics, adjusting an operating voltage or an operating frequency of the machine.

23. (New) The method of claim 22, wherein the multiple performance metrics include an instructions-per-clock cycle metric and a memory references-per-clock cycle metric.

24. (New) The method of claim 22, wherein the performance events are instruction counts and memory references that are simultaneously monitored.

25. (New) The method of claim 22, further comprising the machine simultaneously monitoring multiple performance events from different applications executing on the processor.

26. (New) The method of claim 22, further comprising simultaneously monitoring the multiple performance events using a different counter dedicated to monitor for each performance event.